

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER,
SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING
SEMICONDUCTOR DEVICE

5

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device comprising ^a chip size package ^{of the type used} ^a ~~(using)~~ for high density mounting module, ^a multichip module, and the like, a method
10 of manufacturing ^{the} same, and to ^a semiconductor wafer ~~(using)~~ ^{used} for manufacturing the semiconductor device.

Currently, in accordance with ^{the current trend toward} making electronic devices ^{while retaining a} small ~~[and]~~ high performance, semiconductor devices used therein are required to ^{have a} ~~(be)~~ high integration, ^a high
15 density, and ^{to have a} fast ~~[in a]~~ processing ^{speed} ~~[velocity]~~.

Corresponding to ^{such a} ~~(the)~~ requirement, ~~(implementing)~~ ^{the} ~~the~~ methods of ^{manufacture of} semiconductor devices have been changed from ^{the} pin insertion type to ^a surface implementing method for increasing ^{the} implementing density ~~(i)~~; and, in order to
20 ^{accommodate an} ~~(correspond to)~~ increasing ~~(the)~~ number of pins, packages, such as ^a ~~(from)~~ DIP (Dual Inline Package) ^a ~~(to)~~ QFP (Quad Flat Package), ^a PGA (Pin Grid Array), and the like, have been developed.

However, implementation of the QFP is becoming difficult ^{because of the} ~~(in accordance with)~~ increasing ~~(the)~~ number of pins, ^{since the} ~~(because)~~ connecting leads with ^{the} implementing substrate are concentrated at ^{can be} periphery of the package, and the lead itself is thin and readily deformed. The PGA is
25 disadvantageous in ^a high density implementation, because ^{the}

increasing processing velocity is difficult^{to attain} electrically,
 since terminals of the PGA for connecting with^{the} implementing
 substrate are slender and^{are} concentrated^{so as to be} extremely^{close to} each
 other, and surface implementation is impossible, since the
 5 PGA^{package} is a pin insertion type.

Recently, in order to solve the above problems and to
 realize a semiconductor device [corresponding to] ^{having an}
 [increased] processing velocity, ^a BGA (Ball Grid Array), ^{package} has
 been developed. The BGA^{package} comprises a stress buffer layer
 10 between semiconductor chips and a substrate whereon
 circuits are formed, and bump electrodes, which are
 external terminals, ^{on the} [at] implementing substrate side of the
 substrate whereon circuits are formed (US Patent
 5,148,265). ^A [The] package having ^a [the] BGA structure is
 15 readily implemented ^{the} on surface, because deformation of the
 leads, such as QFP, ^{occurs in a} ^{does} ^{occurs} [is] not [occurred], since the terminals for
 connection with^{the} implementing substrate ^{are provided in the form of} [is] ball-shaped
 solders, and ^{the} [a] pitch between the terminals can be [taken]
 wide, since the terminals^{are} dispersed ^{on} all through the
 20 implementing plane. Furthermore, because the length of
 the bump electrode, i.e. the external terminal, is short
 in comparison with the PGA^{package}, ^{the} inductance component is small, ^{the}
 signal velocity is fast, and it is possible to [correspond]
^{accommodate} [to] the requirement to increase^{the} processing velocity.

25 On the other hand, JP-A-8-172,159 (1996) discloses LOC
 (Lead On Chip) ^{formed} package, which comprises a cross sectional
 composition of sealing material/chip/protecting
 film/sealing material, as ^a [the] chip provided with ^a [the]

protecting film. The protecting film increases^{the} adhesion of the chip with the sealing material, and^{at the same time,} protects the chip from^{damage} ^a [damages] by pick up pin^a, concurrently].

JP-A-7-135189 (1995) discloses an invention relating
 5 to^a wafer adhesion sheet for manufacturing semiconductor devices^{having a} of LOC structure. The wafer adhesion sheet is^{sued} ^{used} as a protecting film until the chip is mounted in a package ^{during the} (in a) process for manufacturing the semiconductor.

Recently, in accordance with widespread^{used} ^{a decrease in} (used) of
 10 portable information terminals, ^a [decreasing] size and high density mounting of semiconductor devices are required. Therefore,^a CSP (Chip Scale Package), the package size of which is almost^{the} same as chip, has been developed. ^A [The] CSP of various types ^{has been} (are) disclosed in "Nikkei Micro Device"
 15 p38-p64, published by Nikkei BP Co. (February, 1998). ^A [Those] CSP (are)^{is typically} manufactured by the steps of: adhering semiconductor chips, which has been cut ^{into} (to) respective pieces, onto a polyimide substrate or ceramic substrate, whereon^a circuit layer is formed; ^{connecting} [connecting] electrically^a
 20 the circuit layer with the semiconductor chip by a method such as wire bonding, single point bonding, gag bonding, bump bonding, and^{the like} [others]; sealing the connecting portion with^a resin; and forming external terminals, such as solder bumps. ^P JP-A-9-232256 (1997) and JP-A-10-27827 (1998)
 25 disclose methods of mass production of ^a (the) CSP. In accordance with^{these} (the) methods, the semiconductor device is manufactured by the steps of: forming bumps on the semiconductor wafer; connecting the circuit substrate

electrically via the bumps; sealing the connecting portions with^a resin; forming the external electrodes on the circuit substrate; and cutting the wafer ^{into} [to] respective pieces. The "Nikkei Micro Device" p164-p167, published by
 5 Nikkei BP Co. (April, 1998), discloses another mass production method ^{for} [of] the CSP. In accordance with the disclosed method, the semiconductor device is manufactured by the steps of: forming bumps on the semiconductor wafer by soldering; sealing portions other
 10 than the bumps with^a resin; forming external electrodes at the bump portions; and cutting the wafer ^{into} [to] respective pieces.

Among the ^{which are} [above] CSP, assembled by adhering the semiconductor chips cut in pieces to ^a [the] polyimide substrate or ^a [the] ceramic substrate, ^a [the] CSP[,] wherein ^a [the] circuit layer is connected to the chip by wire bonding[,] becomes larger than the chip size, naturally, because the bonding area of the circuit layer is located ^{outside} [at exterior] of the chip. In ^{the} case of ^a [the] CSP connected by bump bonding,
 20 the substrate becomes larger than the chip in order to prevent resin from flowing down at ^{the time of} potting, because the interval between the chip and the substrate is sealed with resin after bonding. Accordingly, ^{occurred in} [there was such] a problem ^{such a} that the package size of ^a [these] CSP became larger
 25 than the chip.

^A [The] CSP using ^{experienced} [the] chips cut in pieces had such a problem ^{to manufacture} in that ^{it} [the CSP] took a long time ^{in manufacturing} the semiconductor device, because, after dicing the chips,

each [of] respective chip must be located correctly on the substrate, adhered thereon, connected electrically, and sealed.

5 [The]^A CSP using [the]^a resin substrate, such as, polyimide and the like, as the circuit layer had [such] a problem, that water, absorbed in the package at re-flowing when the package was provided onto the mounting substrate, was expanded and failures, such as bubble formation and peeling off, were generated, because the chip was adhered with an
10 adhering agent.

[The]^A CSP, which was manufactured by the steps of: forming bumps on the semiconductor wafer; connecting the semiconductor wafer with the substrate; sealing the interval between the substrate and the semiconductor wafer
15 with^a resin; forming the external electrodes; and cutting [off] the semiconductor wafer^{into} [to] respective pieces; had [such] a problem [as warp]^{of warping} of the semiconductor wafer and the semiconductor device [by]^{due to} curing shrinkage, because the resin layer was formed^{on} only one side of the wafer.

20 Additionally, except^{for} the wire bonding type CSP, many of the CSP have an exposed plane, which is [in reverse of]^{opposite to} the plane whereon the circuits are formed^{on} [of] the chip.

Therefore, there was a problem^{in that} [to generate] failures, such as cracks at edge of the chip, and [damages at] the rear
25 plane [by] falling down during transportation^{when the package is picked up} of the package, [and handling] such as [picking] up during mounting operation.

SUMMARY OF THE INVENTION

In consideration of the above circumstances, one of the objects of the present invention is to provide semiconductor devices and ^a semiconductor wafer^[i], wherein the package size is ^{the} (as) same as the chip size, and failures in appearance, such as warp and ^{damage} (damages) are scarcely generated^[i], and to provide a method of manufacturing the same.

(Other one of the objects) ^{Another object} of the present invention is to provide to provide semiconductor devices and ^a semiconductor wafer^[i], the package size of which is ^{the} (as) same as the chip size, ^{and which has a} superior ^{in which} (in) mounting reliability and mass producibility, and failures in appearance, such as warp and ^{damage,} (damages), are scarcely generated^[i], and to provide a method of manufacturing the same.

The gist of the present invention to achieve the above objects is featured by ^a (the) semiconductor device comprising a semiconductor chip, a stress relaxing layer provided on ^a (the) plane ^{of the semiconductor chip}, whereon the circuit and electrodes are formed, ^{of the semiconductor chip,} a circuit layer formed on the stress relaxing layer and connected to the electrodes, and external terminals provided on the circuit layer. ^{The semiconductor device} further comprises an organic protecting film provided on ^a (the) plane ^{opposite} (contrary) to the stress relaxing layer of the semiconductor chip.

^{Another} (Other) feature of the present invention ^{resides} (is) in ^a (the) semiconductor device comprising a semiconductor chip, a porous stress relaxing layer provided on ^a (the) plane ^{of the semiconductor chip}, whereon the circuit and electrodes are formed, ^{of the semiconductor} (chip,) a circuit layer formed on the stress relaxing layer

and connected to the electrodes, and external terminals provided on the circuit layer^{. The semiconductor chip} further comprises an organic protecting film provided on^a the plane^{opposite} [reverse] to the stress relaxing layer of the semiconductor chip, and respective

5 [of] side planes of the stress relaxing layer, the semiconductor chip, and the organic protecting film (is)^{are} exposed outside on a same plane.

^{Another} [Other] feature of the present invention^{resides} (is) in (the)^a semiconductor device comprising a semiconductor chip, a porous stress relaxing layer provided on^a the plane^{of the semiconductor chip} whereon the circuit and electrodes are formed [of the semiconductor chip], a circuit layer formed on the stress relaxing layer and connected to the electrodes, an anisotropic conductor for electrical connection provided between the electrodes

10 on the semiconductor chip and the circuit layer, external terminals provided at designated locations on the circuit layer in a grid array shape⁽ⁱ⁾ and an organic protecting film provided on^a the plane^{opposite} [reverse] to the plane^{of the semiconductor chip} whereon the circuit and the electrodes are mounted [of the

15 (semiconductor chip)^{and}; wherein, respective (of) side planes of the stress relaxing layer, the semiconductor chip, and the organic protecting film (is)^{are} exposed outside on (a)^{the} same plane.

^{Another} [Other] feature of the present invention^{resides} (is) in (the)^a semiconductor wafer comprising^a plurality of chip areas, each of which comprises^a circuit and electrodes; ^a a stress relaxing layer provided on^a the plane⁽ⁱ⁾ whereon the circuit and electrodes in the chip area are formed; a circuit layer

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formed on the stress relaxing layer and connected to the electrodes; ^{and} external terminals provided on the circuit layer; ^{and} further comprises ^a an organic protecting film provided on ^a the plane ^{opposite} [reverse] to the stress relaxing layer

5 in the chip area.

^{Another} ^{resides} [Other] feature of the present invention ^a [is] in ^a the method ^a [for] manufacturing semiconductor device comprising the steps of: forming ^a the stress relaxing layer on ^a the plane ^a [whereon] the circuit and electrodes are formed ^a [of the] ^a respective chip area of ^a the semiconductor wafer; forming an organic protecting film on ^a the plane ^{opposite} [reverse] to the plane ^a [whereon] the electrodes are formed ^a [of the] respective chip area; forming via-holes in the stress relaxing layer on the chip area; forming conductors in the via-holes; forming ^a circuit on the stress relaxing layer; forming ^a the external terminals on the circuit layer; and cutting the chip area, the substrate having the circuit, and the organic protecting film at the same plane so as to ^a [be] provide minimum units for operating the semiconductor device

10 20 obtained by the cutting.

On the semiconductor wafer ^{according to} [disclosed in] the present invention ^a plurality of chip areas are arranged regularly; the chip area ^{provides a} [is the] minimum unit circuit for operating the semiconductor device, comprising semiconductor

25 circuits such as logic ^a memory ^a gate array, and the ^{like} others, and the electrodes for input/output of electric signals ^{to the} [with] outside the semiconductor wafer. The electrodes of the semiconductor device are arranged in a manner indicated

in FIG. 11.

In accordance with the present invention, the substrate provided with ^a(the) circuit layer is composed of ^a(the) porous stress relaxing layer and the circuit layer, whereon the circuits are formed. The porous body is composed of a body comprising a structure of continuous bubbles having many fine pores inside, or a three dimensional ^{network}(net work) structure having ^abreathing property. The porous body is formed by any one of: a track etching method, wherein the member is irradiated by neutrons and etched by a chemical agent; a drawing method, wherein ^acrystalline polymer is heated or plasticized with a plasticizer, and, subsequently, the crystalline polymer is drawn; a dissolution layer separating method, wherein a solvent having ^adifferent solubility depending on temperature is used; an extraction method, wherein a polymer is mixed with an inorganic salt, silica, and ^{other materials}(others) uniformly, and after forming a film, only the inorganic salt, and silica are extracted; a layer transferring method, wherein a polymer, a good solvent, and a poor solvent are mixed together, and after forming a film, only the good solvent is evaporated; and ^{other methods}(others). Additionally, ^anon-woven fabric, a sheet of which is formed by a paper machine using polymers polymerized in a solvent in a fibrous state, is included. The ^{term}breathing property ^{refers to}(means) a phenomenon ^{in which}(that) a gas, such as steam, air, and ^{other gas}(others) passes through the porous body via fine pores existing inside the porous body.

In accordance with the present invention, the linear expansion coefficient of the protecting film is preferably close to the linear expansion coefficient of the adhesion layer for adhering the stress relaxing layer ^{to} ~~(with)~~ the semiconductor chip. The warp of the semiconductor chip and the semiconductor wafer by thermal stress can be prevented by making the difference of the linear expansion coefficient of the organic protecting film from those of the stress relaxing layer and the adhesion layer small.

10 ^{the thickness} [Thickness] of the protecting film is ^{greater} ~~[thicker]~~ th ~~than~~ thickness of passivation film, such as PIQ formed on the plane, whereon the circuits are formed, and thinner than the thickness of the chip. After back grinding the rear plane of the wafer, the protecting film can be formed by adhering a sheet

15 of the protecting film to the back ground plane of the semiconductor wafer, or coating the plane with a varnish made of the protecting film material by ^a spin coating method. The protecting film is adhered tightly to the wafer. The protecting film is desirably colored with black for

20 shielding light.

In accordance with the present invention, the porous relaxing layer can be made of polycarbonate, polyester, aromatic polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride,

25 cellulose acetate, polysulfone, polyacrylonitrile, polyamide, aromatic polyamide polyimide, aromatic polyimide, and their compounds. A part of the relaxing layer may be formed of a photosensitive material. The

relaxing layer is more porous than the protecting film.

The circuit layer can be formed with any of gold, copper, aluminum, and these conductors, the outer surface of which^{is} plated with gold. [These]^{this} circuit layer can be the

5 insulating substrate, whereon the circuits are formed with one of these conductors. The insulating substrate is desirably made of engineering plastics superior in heat resistance and mechanical characteristics, such as polyimide and the like.

10 The circuit layer is manufactured by forming the conductor layer directly on the relaxing layer by vapor deposition or plating and the like, and, subsequently,^{by} forming the circuits by etching the conductor layer.

Otherwise, the circuit layer can be formed by adhering the
15 insulating substrate, whereon the circuit^{is} (are) formed with the conductor, onto the stress relaxing layer. The

adhering agent is composed of any resin of epoxy, maleimide, phenol, cyanate, polyamide, polyimide, polyamide-imide, polyester, polyolefin, polyurethane,
20 and the like, and a mixture of any of these resins with^a

rubber component, such as silicone rubber, nitrile-butadiene rubber, and the like. Additionally, any agent, which exerts an adhesion force by heating, drying, pressurizing, photo-irradiation, and^{other techniques} others, can be used

25 as the adhering agent. In addition to the above compounds, the adhering agent can be a sheet, which is formed by impregnating any of the above compounds into a core material, such as^a porous body, glass cloth and the like.

The substrate, whereon the circuits are formed, is adhered to the semiconductor wafer with the above adhering agent.

The circuit layer is formed by the steps of: forming the porous relaxing layer on the electrode side plane of the semiconductor wafer; and forming the conductor layer on the relaxing layer by a method such as adhesion, plating, vapor deposition, and ^{other techniques} [others]. Sometimes, the circuit layer is formed by pattern-etching the conductor layer with a designated process.

The via-hole formed between the circuit layer and the semiconductor wafer is manufactured ^{using a} (by) laser, ^a such as He-Ne laser, Ar laser, YAG laser, carbon dioxide gas laser, and the like. Additionally, in some cases, the portions of the relaxing layer corresponding to the electrodes and the circuit layer of the semiconductor wafer are formed with a photosensitive material, and the via-hole is formed by exposing, developing, and etching of the photosensitive material.

The conductor portion for ^{connecting} [connecting] electrically the semiconductor wafer and the circuit layer is formed with a conductive resin made by mixing conductive fine powder, such as carbon, graphite powder, gold, silver, copper, nickel, copper plated with silver, glass plated with silver, and the like, into a resin group binder, ^a such as ^a epoxy group resin, ^a silicone group resin, ^a polyimide group resin, and the like. Electrical conduction can be achieved by forming a plated film in the via hole with ^a metal such as copper ^{using a} (by) plating method. Additionally, the

conductive portion can be manufactured by forming a deposition film on the inner wall of the via-hole with metal such as gold, copper, and others by heating deposition or sputtering deposition in^a vacuum. Other than the above method, in some^{cases} [case], the wafer is [connected] electrically^{connected} with the circuit layer by arranging a material having^{an} anisotropic conduction in a direction of^{the} thickness between the semiconductor wafer and the terminals of the circuit layer. (The)^A material having anisotropic conduction is [such]
 10 a material manufactured by forming through holes with 20 - 30 μ m pitch in an insulation film, such as polyimide and the like, and filling the through holes with a conductive material, such as copper and the like. The material is conductive only when the electrode exists at
 15 the same position in the thickness direction, and^{is} not conductive in the XY direction.

The external electrode to be formed on the substrate, whereon the circuit layer is formed, is a conductor [connecting] electrically^{connecting} the semiconductor device by
 20 melting with heating. Practically, any^{type} of a soldering alloy containing tin, zinc, and lead, silver, copper, or gold, or these metals formed in a ball shape and coated with gold, can be used for connecting the semiconductor device by heating and melting, or contacting and vibrating
 25 without melting. Other than these^{materials} [material], any one of molybdenum, nickel, copper, platinum, titanium, and others, or an alloy composed of at least two of these elements, or a double film structure formed by at least

two of these elements, can be used as the terminal.

The mounting substrate used for the semiconductor module is composed of ^athe₁ conductive layer and ^{an}the_A insulating layer. The insulating layer is composed of_A
 5 resin, such as epoxy, maleimide, phenol, cyanate, polyamide, polyimide, polyamide-imide, polytetrafluoroethylene, and the like, a copolymer of these ^{resins}resin, or a rubber component, such as silicone rubber, nitrile-butadiene rubber, and the like. In particular,
 10 one of the above ^{resins to which a}resin added with ^{is added}photosensitivity, which can be made ^{by}patterning ^{using}by a process such as exposing and developing, is preferable. Furthermore, in addition to the above resin itself, the insulating layer can be formed by impregnating any of the above compounds into a core
 15 material, such as ^aporous body, ^aglass cloth and the like.

The conductive layer is composed of ^ametal, such as gold, copper, aluminum, and the like. In consideration of ^{the}electrical characteristics, the mounting substrate is desirably a substrate ^awhereon a ground layer and a power
 20 supply layer are provided.

In accordance with the present invention, the CSP having a package size ^{which is the}(as) same as the chip size can be provided. ^AThe porous stress relaxing layer is used. The porous body is cut simultaneously when the semiconductor wafer is cut.
 25 Its end plane is inevitably exposed at ^{the}side plane of the package. Therefore, absorbed moisture at reflowing in mounting is released outside passing through the porous body. Accordingly, failures such as peeling off by vapor

pressure of water can be prevented, and ^athe CSP having a high reliability can be provided. Because the wafer is cut altogether ^{into} pieces ^{representing} of respective ^{units} unit after assembling by wafer level, ^athe CSP having a preferable mass producibility can be provided. Furthermore, ^athe CSP ^{can be provided} wherein the warp generated by thermal stress is made small ^{due to} (by) the protecting film formed on ^arear plane of the semiconductor wafer, and appearance failures, such as cracks and damages of the semiconductor chip during handling ^{of} the package, such as ^{during} transportation and ^{positioning} others ^{will be} is scarcely generated ^{can be provided}.

BRIEF DESCRIPTION OF THE DRAWINGS

^{FIGS. 1(a) to 1(i) are}
 (FIG. 1 is a set of) schematic cross sections indicating
 15 manufacturing steps of ^athe semiconductor device ^{representing} in one of
 the embodiment of the present invention;

FIG. 2 is a perspective view of the semiconductor wafer based on the present invention ^{as} obtained by the manufacturing steps indicated in (FIG. 1, FIGS. 1(a) to 1(i);

^{FIGS. 3(a) to 3(h) are}
 20 (FIG. 3 is a set of) schematic cross sections indicating manufacturing steps of ^athe semiconductor device ^{representing another} in the other embodiment of the present invention;

FIG. 4(a) is a schematic cross section and FIG. 4(b) is a perspective view showing
 (FIG. 4 indicates) an example of semiconductor device ^{representing another} in the other embodiment of the present invention, and;

25 (indicates (a) a schematic cross section, and (b) a perspective view,

^{FIG. 5(a) is a schematic cross section and FIG. 5(b) is a perspective view showing}
 (FIG. 5 indicates) an example of semiconductor device in the other embodiment of the present invention, and;

indicates (a) a schematic cross section, and (b) a

perspective view,

FIGs. 6(a) and 6(b) are illustrations
 FIG. 6 is a set of perspective views indicating a part
the of manufacturing steps of ^athe semiconductor device [in the]

5 [other embodiment of] the present invention[.];

FIG. 7(a) is a schematic cross section and FIG. 7(b) is a perspective view showing
 FIG. 7 indicates an example of semiconductor module

based on the present invention, and indicates (a) a

[schematic cross section, and (b) a perspective view,]

showing
 FIG. 8 is a schematic cross section indicating an
a example of semiconductor device ^{representing} [of] a comparative example[.];

showing
 FIG. 9 is a schematic cross section indicating an
a example of semiconductor device ^{representing} [of] a comparative example[.];

showing
 FIG. 10 is a schematic cross section indicating an
a example of semiconductor device ^{representing} [of] a comparative example[.];

15 and

FIGs. 11(a) to 11(c) are diagrams showing
 FIG. 11 is a schematic illustration indicating the
 arrangement of electrodes on the semiconductor chip used
 in the present invention.

20 DETAILED DESCRIPTION OF THE EMBODIMENTS

Hereinafter, embodiments of the present invention ^{will be} (are) ^{with reference to the} explained in detail [referring] to drawings.

(Embodiment 1)

FIGs. 1(a) to 1(c) illustrate in the manufacture of a
 25 FIG. 1 indicates manufacturing steps ^{representing} [of] semiconductor
 device [in] an embodiment of the present invention, and a
 semiconductor device obtained by the manufacturing steps ^{is shown in FIG. 1(c)}

FIGs. 1
 In accordance with the manufacturing steps of (a) ~ 1

(i), the semiconductor wafer and the semiconductor device of the present invention were prepared.

In the step of FIG. 1
 5 (a) [As the insulating substrate ^a1], polyimide film (UB rex S: made by Ube Kosan Co.) [of] 50 μ m thick, whereon an epoxy group adhesive agent was applied, ^{as the insulating substrate} was used. Device holes were formed by punching ⁱⁿ the insulating substrate 1. Electrolytic copper foil [of] 18 μ m thick was adhered to the polyimide film by heating and pressurizing with a roller at 150 °C. After applying photosensitive resist
 10 (P-RS300S: made by Tokyo Ohka Co.) onto the electrolytic copper foil, ^{it was} baked at 90 °C for 30 minutes, and ^{an} [the] etching mask was prepared by exposing and developing ^a [the] pattern.

Then, the copper was etched with ^a ferric chloride aqueous solution (ferric chloride concentration is 40°
 15 Baume: specific gravity; approximately 1.38) at 40 °C, and ^a copper circuit was prepared by peeling off the resist. The circuit 2 was prepared by plating the circuit portion with electrolytic gold. As explained above, ^a [the] circuit 2 corresponding to respective [of plural] chip areas on the
 20 semiconductor wafer was prepared.

In the step of FIG. 1
 (b) ^a [An] adhesive varnish containing ^a non-volatile component 30 % (bisphenol A type epoxy resin (EP1010: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ^a ortho-cresol novolak type phenol
 25 hardener (H-1: made by Meiwa Kasei Co.) was added, and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) was mixed) was applied onto one of ^{the} surfaces of ^a [the] porous body ^a 3(i) composed of polyimide non-woven cloth having three

dimensional network structure of $150 \mu\text{m}$ and (dried) the
was then dried
 varnish. By adhering the circuit layer 2 prepared by the
of FIG 1
 manufacturing step (a) to the porous body 3 *using an* via the adhesive
 agent by heating and pressurizing at 120°C for 5 seconds,

5 the substrate comprising the circuit layer was prepared.

In the step of FIG 1
 1 (c) *the* (The) substrate, whereon the circuit layer was
 formed, the adhesive agent 4, the semiconductor wafer 6,
 and the wafer protecting film 7 were arranged as indicated
 (in FIG. 1). The substrate 1, whereon the circuit layer was
 10 formed, and the electrode 5 on the wafer were adjusted *in* (their) *in*
 position to match each other. As the semiconductor wafer
 6, a semiconductor wafer *in diameter* (of) 4 inches and $525 \mu\text{m}$ thick was
 used.

The adhesive agent 4 and the wafer protecting film 7
 15 were prepared by impregnating *an* (the) adhesive varnish
 containing *a* non-volatile component 35 % (biphenyl type
 epoxy resin (YX-4000: made by Yuka Shell Co.) was
 dissolved into a solvent, i.e. methylethylketone, *a*
 ortho-cresol novolak type phenol hardener (H-1: made by
 20 Meiwa Kasei Co.) was added, and *a* micro-filler having *a* primary
 particle size of 12 nm (R974: made by Nippon Aero sol Co.)
 and a catalyst (triphenylphosphine: made by Wako Jyunyaku
 Co.) were mixed) into the polyimide non-woven cloth of 30
 μm and *was dried* (drying) the varnish.

In the step of FIG. 1
 25 1 (d) *after* (After) back grinding the rear plane of the
 semiconductor wafer 6 to expose the silicon, the above
 members were adhered to the rear plane of the wafer by
 heating and pressurizing at 120°C for 5 seconds.

Furthermore, the members were cured by heating at 170 °C for 60 minutes.

In the step of FIG. 1
1 (e), [The] via-holes 8 of 50 μ m in diameter were formed by^a YAG laser (made by ESI Co., wavelength: 355 nm, peak
5 power: 4 kW, energy: 200 μ j, pulse width: 50 ns).

In the step of FIG. 1
1 (f) [The] ^{the}conductor portion 9 was formed by injecting conductive paste (GP913: made by Asahi Kasei Co.) into the via-holes 8 ^{using} [by] a printing method, and heating and curing^{the conductive paste} at 170 °C for 40 minutes.

In the step of FIG. 1
10 (g) [The] ^{the}external electrode 10 was formed by applying flux at solder ball connecting portions of the substrate 1, whereon the circuit layer was formed, placing^a eutectic solder ball (Pb 63: Sn 37) of 0.6 mm [in] diameter thereon, and heating the solder ball by infrared re-flow heating
15 at 240 °C for 5 seconds. Finally, marking was performed on the wafer protecting film 7 with an ink jet printer.

In accordance with the above manufacturing steps, the semiconductor wafer 6, whereon plural chip areas were formed as indicated in FIG. 2, was prepared. The amount
20 of warp of the semiconductor wafer 6 was evaluated^{using a} [by] film thickness measuring profilometer (dectac: made by ULVAC Co.).

In the step of FIG. 1
1 (h) [In] ⁱⁿorder to cut the semiconductor wafer 6, dicing tape (UE-111AJ: made by Nitto Denko Co.) was adhered onto
25 the rear plane of the wafer protecting film 7. Then, a dicing saw [of] 200 μ m thick was attached to a dicer (DAD520: made by Disco Co.), and the substrate 1, whereon the circuit layer was formed, the adhesive agent 4, the semiconductor

wafer 6, and the wafer protecting film 7 were cut simultaneously ^{on the} [at a] same plane, so that the semiconductor device 17, obtained by cutting the semiconductor wafer 6, ^{represent the smallest} would [be an] operable [smallest] unit, i.e. the chip 64.

- 5 After cutting, the dicing tape was peeled off from the wafer protecting film.

FIG 1 shows the

- 1 (i) ^{as} (The) semiconductor device 17 of the present invention ^{by the steps} (was) prepared (as) explained above. The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test ^{to detect} (such as) ^a generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate [of] 5 mm thick.
- 20 Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in following Table 1.

Table 1

		Amount of warp of wafer(μ m)	Amount of warp of package(μ m)	Failure generation rate after 1000 cycles* ¹ (Number of failures/number of tests)	
5	E-1	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	E-2	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	10	E-3	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100
		E-4	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100
		E-5	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100
		E-6	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100
15	E-7	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	E-8	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	E-9	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	E-10	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
	E-11	$\leq 5 \mu$ m	$\leq 1 \mu$ m	0/100	
20	C-1	-	5μ m	85/100	
	C-2	-	$\leq 1 \mu$ m	20/100* ³	
	C-3	20μ m	5μ m	20/100	

*1: Number of breakage (failures) after 1000 cycles in the range from -55°C to -125°C .

*2: Number of failures such as peeling, bubbling etc. during an infrared reflow test, after leaving the chip in an atmosphere of relative humidity of 85 % at 85°C for 166 hours.

*3: Breakage failures between chip/circuit substrate.

*4: Generation of breakage or cracks in ^achip when dropping ^{the chips} from 1 meter high ^{onto a} (to) glass substrate [of] 5 cm thick was determined as ^a failure.

5

Table 1 (continued)

		Failure generation rate in reflow test* ² (Number of failures/number of tests)	Failure generation rate in dropping test* ⁴ (Number of failures/number of tests)	Ratio of area (package area/chip area)
10	E-1	0/100	0/20	1
	E-2	0/100	0/20	1
15	E-3	0/100	0/20	1
	E-4	0/100	0/20	1
	E-5	0/100	0/20	1
	E-6	0/100	0/20	1
	E-7	0/100	0/20	1
20	E-8	0/100	0/20	1
	E-9	0/100	0/20	1
	E-10	0/100	0/20	1
	E-11	0/100	0/20	1
	C-1	90/100	0/20	1.44
25	C-2	0/100* ³	8/20	1.2
	C-3	50/100	12/20	1

*1: Number of breakage (failures) after 1000 cycles in the

range from -55 °C to -125 °C.

*2: Number of failures such as peeling, bubbling etc.

during ^{an} infrared reflow test, after leaving ^{the chip} in ^{an atmosphere of} relative humidity ^{of} 85 % at 85 °C for 166 hours.

5 *3: Breakage failures between chip/circuit substrate.

*4: Generation of breakage or cracks in ^a chip when dropping ^{the chip} from 1 meter high ^{onto a} [to] glass substrate [of] 5 cm thick was determined as ^a failure.

10 The semiconductor wafer 6 prepared in the present embodiment had a ^{small} warp [as small as] equal to or less than 5 μ m. The semiconductor device prepared in the present embodiment 17 had a small warp. The conductor portion can be made of a low coefficient of elasticity by connecting

15 the chip 64 to the circuit layer 2 with a conductive resin, and the semiconductor device is made superior particularly in thermal cycle resistance, in addition to the effect of the stress relaxing layer. In accordance with the porous stress relaxing layer, reflow failure in mounting is not

20 generated. The failure such as damage of the chip is not generated in the dropping test. The package size can be made ^{the} [as] same as the size of ^{the} chip. In accordance with the process of the present embodiment, the package can be made ^{merely} [only] ^{so} by dicing, and it is superior in mass producibility.

25

(Embodiment 2)

^{FIGs. 3(a) to 3(h) show} ^{in the manufacture of a} ^{representing another} ^{device} [FIG. 3 indicates manufacturing] steps [of] semiconductor device [in the other] embodiment of the present invention,

and a semiconductor device obtained by the manufacturing steps is shown in FIG. 3(h).

In accordance with the manufacturing steps of FIGs 3 (a) ~ 3 (h), the semiconductor wafer 6 and the semiconductor

5 device 17 of the present invention were prepared.

in the step of FIG. 3 (a) (The)^a porous body 3 made of polytetrafluoroethylene having a three dimensional network structure of 150 μ m, which was prepared by a drawing method, the adhesive agent 4, the semiconductor wafer 8, and the wafer protecting film 7 were arranged as indicated in FIG. 3. (The)^A semiconductor wafer 8 (of)^{which was} 4 inches in diameter and 525 μ m in thickness, was used. The adhesive agent 4 and the

10 wafer protecting film 7 were prepared by impregnating the adhesive varnish containing non-volatile component 35 % (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e.

methylethylketone,^{an} ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and^a micro-filler having primary particle size of 12 nm (R974: 20 made by Nippon Aero sol Co.) and a catalyst

(triphenylphosphine: made by Wako Jyunyaku Co.) were mixed into the polytetrafluoroethylene sheet having a three dimensional structure of 30 μ m^{was dried}, and (drying) the varnish. After back grinding the rear plane of the 25 semiconductor wafer 6 so as to remove SiO₂ and to expose^{the} silicon, the above members were adhered by heating and pressurizing at 120 °C for 5 seconds. Furthermore, the members were cured by heating at 170 °C for 60 minutes.

In the step of FIG 3

1 (b) (The) via-holes 8 of 50 μ m in diameter were formed by YAG laser (made by ESI Co., wavelength: 355 nm, peak power: 4 kW, energy: 200 μ J, pulse width: 50 ns).

In the step of FIG 3

2 (c) (The) plated^a 12 was formed by immersing the
5 semiconductor wafer, wherein the via-holes were formed in the porous body, backed by the wafer protecting film, into a plating solution at 70 °C to perform an electroless copper plating. Before plating, the semiconductor wafer was immersed into an acidic solution of^a sensitizer (HS101B: made by Hitachi Kasei Co.) for treating^a catalyst of catalytic electroless copper plating. The plating solution used had a composition of: copper sulfate heptahydrate; 0.04 mole/liter, ethylenediamine tetraacetic acid dihydrate; 0.1 mole/liter, glyoxylic
15 acid; 0.03 mole/ liter, sodium hydroxide; 0.1 mole/liter, 2, 2'pyridyl; 0.0002 mole/liter, and polyethylene glycol; 0.03 mole/liter.

In the step of FIG 3

3 (d) (An) etching mask was prepared by applying
photosensitive resist (P-RS300S: made by Tokyo Ohka Co.)
20 onto the copper plated film, baking^{the resist} at 90 °C for 30 minutes, and exposing and developing the pattern. Then, the copper was etched with ferric chloride aqueous solution (ferric chloride concentration is 40° Baume: specific gravity; approximately 1.38) at 40 °C, and^a copper circuit was
25 prepared by peeling off the resist. The circuit 2 was prepared by plating the circuit portion with electrolytic gold.

In the step of FIG 3

4 (e) (The) solder resist film 13, whereon lands for

external terminals were formed, was prepared using a photosensitive solder resist agent (PSR4000: made by Taiyo Ink Co.) on the circuit 2. The solder resist agent was applied onto the circuit side of the wafer by spin coating ^a and the agent was ^{then exposed} method, ^{developed} dried at 80 °C for 20 minutes, and ^{then exposed} [exposing] and [developing] to form the lands. Further, it was cured at 150 °C for 60 minutes.

In the step of FIG. 3 1(f) ^{on} [The] external electrode 10 was formed by applying flux at the land portions, placing ^a eutectic solder ball (Pb 63: Sn 37) [of] 0.6 mm in diameter thereon, and heating the solder ball by infrared re-flow heating at 240 °C for 5 seconds. Finally, marking was performed on the wafer protecting film 7 formed on the rear plane of the semiconductor wafer with an ink jet printer.

15 In accordance with the above manufacturing steps, the semiconductor wafer 6, whereon plural chip areas 62 were formed as indicated in FIG. 2, was prepared. The amount of warp of the semiconductor wafer 6 was evaluated ^{using a} (by) film thickness measuring profilometer (dectac: made by ULVAC Co.).

In the step of FIG. 3 1(g) ^{in the wafer} [In] order to cut, dicing tape 120 was adhered onto the wafer protecting film 7. A dicing saw 11 ^{which was} [of] 200 μm thick, was attached to a dicer (DAD520: made by Disco Co.), and the substrate 1, whereon the circuit layer was formed, 25 the adhesive agent 4, the semiconductor wafer 6, and the wafer protecting film 7 were cut simultaneously ^{on the} (at a) same plane so that the semiconductor device 17, obtained by cutting the semiconductor wafer 6, would ^{represent the smallest} be an operable

[smallest] unit, i.e. the chip 64. After cutting, the dicing tape was peeled off from the wafer protecting film.

FIG 3

1 (h) ^{shows the} [The] semiconductor device 17 of the present invention ^{as by the steps} [was] prepared [as] explained above. The
 5 semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a
 10 reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test
 [such as] ^{to determine} generation of ^a chip crack and the like was performed after dropping the semiconductor device at a
 15 height of 1 meter ^{onto} [on] a glass plate [of] 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 ^{represented by} [prepared in] the present
 20 embodiment had a ^{small} warp [as small as] equal to or less than 5 μm. The semiconductor device prepared in the present embodiment 17 had a small warp, and the semiconductor device is superior particularly in thermal cycle resistance, because the stress relaxing layer is made of
 25 porous polytetrafluoroethylene having a low coefficient of elasticity. The semiconductor device does not generate ^a reflow failure ^{during the} [at] mounting operation, because it is a low humidity absorber. Because the chip can be connected

electrically with the circuit layer by forming the conductors at the via portions and the circuit layer simultaneously by plating, the semiconductor device of the present invention is superior in mass producibility.

5 ^A
 [The] failure, such as damage ^{to} [of] the chip ^{was} [is], not generated in the dropping test. The package size can be made ^{the} [as] same as the size of ^{the} chip. In accordance with the process of the present embodiment, the package can be made ^{merely} [only] by dicing the semiconductor wafer of the present
 10 embodiment, and the process is superior in mass producibility. In accordance with the process of the present embodiment, adjusting ^{the} locations of the circuit layer and the pads on the chip becomes unnecessary, and the manufacturing process can be simplified.

15

(Embodiment 3)

FIG. 4(a) and FIG. 4(b) ^{show} [indicate] a cross sectional view and a perspective view ^{, respectively,} of ^a [the] semiconductor device ^{representing another} [in the other] embodiment of the present invention,]
 20 [respectively]. The semiconductor device was obtained by the following manufacturing steps.

After forming the via-holes by the same process as the embodiment 2, copper film was formed on the inner wall of the via-holes and the surface of the porous body by a vacuum
 25 deposition method. The subsequent processes were ^{the used in} [performed as] same as the previous embodiment to manufacture the semiconductor wafer 6 and the semiconductor device 17.

The semiconductor device 17 was mounted on a mounting

substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used.

5 Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test ^{to detect} [such as] generation of ^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} [on] a glass plate ^{of} [of] 5 mm thick.

10 Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 ^{of} [prepared in] the present embodiment had a ^{small} warp [as small as] equal to or less than 5 μm. The semiconductor device 17 ^{of} [prepared in] the present embodiment had a small warp, and the semiconductor device is superior particularly in thermal cycle resistance, because the stress relaxing layer is made of porous

20 polytetrafluoroethylene having a low coefficient of elasticity. The semiconductor device does not generate ^a reflow failure ^{during the} [at] mounting operation, because it is a low humidity absorber. Because the conductive portions are formed by ^a [the] vapor deposition, ^{the} [the] conductive layer having

25 a high purity can be formed, and ^{the} electrical resistance is decreased. Therefore, the semiconductor can ^{accommodate} [correspond] ^A (to) increasing ^{speed} (velocity) of ^{operation} electrical signals. ^{was} [The] failure, such as damage of the chip ^{is} [is] not generated in the dropping

test. Furthermore, the package size can be made ^{the} [as] same
 as the size of the chip, and the package can be made ^{merely} [only]
 by dicing the semiconductor wafer of the present embodiment.
 Therefore, the process is superior in mass producibility.

5

(Embodiment 4)

FIG. 5(a) and FIG. 5(b) ^{show} [indicate] a cross sectional
^{, respectively, a}
 view and a perspective view of ^a [the] semiconductor device
^{representing another}
 [in the other] embodiment of the present invention,
 10 [respectively]. The semiconductor device 17 was obtained
 by the following manufacturing steps.

As the porous body 3, porous polyimide ^{and} [of] 120 μ m thick,
 having a three dimensional network structure, which was
 prepared by a layer transfer method, was used. As the
 15 adhesive agent and the wafer protecting film,
 thermoplastic polyimide (TP-D: made by Kaneka Co.) [of] 30
 μ m thick was used, and the semiconductor wafer and the
 semiconductor device were prepared by the same method as
 the embodiment 1. However, heating and pressurization for
 20 adhering layers was performed at 260 °C for one second.

The semiconductor device 17 was mounted on a mounting
 substrate, and a temperature cycle test in the range from
 -55 °C to -125 °C was performed. As the mounting
 substrate, a copper clad glass cloth base epoxy laminate
 25 FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used.
 Furthermore, a reflow test at 240 °C for 5 seconds was
 performed after absorbing moisture in an environment at
 85 °C and a relative humidity of 85 % for 48 hours. An

appearance test ^{to detect} [such as] ^a generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} [on] a glass plate ^{of} [of] 5 mm thick. Furthermore, the package area versus chip area was
 5 evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment had ^{small} a warp [as small as] equal to or less than 5 μ m. The semiconductor device 17 ^{of} [prepared in] the present
 10 embodiment had a small warp. The semiconductor device is superior particularly in thermal cycle resistance, because the conductive portions could have a low coefficient of elasticity by connecting the chip to the circuit layer with ^a conductive resin, in addition to the
 15 effect of the stress relaxing layer. The semiconductor device does not generate ^a reflow failure ^{during the} [at] mounting operation, because of the porous stress relaxing layer. ^A [The] failure, such as damage ^{to} [of] the chip ^{was} [is] not generated in the dropping test. Furthermore, the package size can
 20 be made ^{the} [as] same as the size of the chip, and the package can be made ^{merely} [only] by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

25 (Embodiment 5)

^A [The] semiconductor device 17, which was the same type ^(a) as indicated in FIG. 4, was prepared by the following manufacturing steps.

As the porous body 3, porous polyimide^{and} [of] 120 μ m thick^A having a three dimensional network structure, which was prepared by a layer transfer method, was used. As the adhesive agent and the wafer protecting film,^a
 5 thermoplastic polyimide (TP-D: made by Kaneka Co.) [of] 30 μ m thick was used, and the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same method as the embodiment 2.

The semiconductor device 17 was mounted on a mounting
 10 substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was
 15 performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test [such as] ^{to detect} generation of^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} [on] a glass plate [of] 5 mm thick.
 20 Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 ^{small} [prepared in] ^{of} the present embodiment has a warp [as small as] equal to or less than
 25 5 μ m. The semiconductor device 17 ^{of} [prepared in] the present embodiment has a small warp and superior thermal cycle resistance, and does not generate^a reflow failure (at) ^{during the} mounting operation. Because the chip can be connected

electrically with the circuit layer by forming the conductors at the via portions and the circuit layer simultaneously by plating, the semiconductor device of the present invention is superior in mass producibility.

5 ^A
 [The] failure, such as damage ^{to} [of] the chip ^{was} [is] not generated in the dropping test. The package size can be made ^{the} [as] same as the size of chip. In accordance with the process of the present embodiment, the package can be made ^{merely} [only] by dicing the semiconductor wafer of the present embodiment,
 10 and the process is superior in mass producibility.

(Embodiment 6)

15 ^A
 [The] semiconductor device 17, which was the same type as indicated in FIG. 4, ^(c) was prepared by the following manufacturing steps.

As the porous body 3, porous polyimide [of] 120 μ m thick ^{and} having a three dimensional network structure, which was prepared by a layer transfer method, was used. As the adhesive agent and the wafer protecting film,
 20 thermoplastic polyimide (TP-D: made by Kaneka Co.) [of] 30 μ m thick was used, and the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same method as the embodiment 3.

25 The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used.

Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test (such as) ^{to detect} generation of ^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} [on] a glass plate [of] 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

10 The semiconductor wafer 6 [prepared in] ^{of} the present embodiment has a ^{small} warp [as small as] equal to or less than 5 μm. The semiconductor device 17 [prepared in] ^{of} the present embodiment has a small warp and superior thermal cycle resistance, and does not generate ^a reflow failure (at) ^{during} the mounting operation. Because the conductive portions are formed by ^a [the] vapor deposition, ^{the} [the] conductive layer having a high purity can be formed, and ^{the} electrical resistance is decreased. Therefore, the semiconductor can ^{accommodate} [correspond] ^{an} (to) increasing ^{speed} [velocity] of ^{operation} electrical signals. ^A [The] failure, such as damage ^{to} [of] the chip ^{was} [is] not generated in the dropping test. Furthermore, the package size can be made [as] ^{the} same as the size of the chip, and the package can be made ^{only} [only] ^{manually} by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

25

(Embodiment 7)

^A (The) semiconductor device 17, which was the same type ^(a) as indicated in FIG. 5, ^{was} prepared by the following

manufacturing steps.

The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 1 using^{an} alamide non-woven cloth (thermount: made by Du Pont Co.)
 5 [of] 100 μ m thick as the porous body [3]; and a sheet made of rubber modified epoxy resin [of] 30 μ m thick as the adhesive agent and the wafer protecting film. The adhesive sheet was prepared by^{dissolving} [applying] a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) [was]
 10 [dissolved] into a solvent, i.e. methylethylketone,^{an} ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and^a micro-filler having^a primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei
 15 Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) onto^a bed-film, and [drying]
 the varnish.^{was dried}

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from
 20 -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at
 25 85 °C and a relative humidity of 85 % for 48 hours. An appearance test^{to detect} (such as)^a generation of^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter^{onto} (on) a glass plate [of] 5 mm thick.

Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 (prepared in^d) the present embodiment has a ^{small}warp (as small as) equal to or less than 5 μ m. The semiconductor device 17 (prepared in^d) the present embodiment has a small warp. The semiconductor device is superior particularly in thermal cycle resistance, because the conductive portions could have a low coefficient of elasticity by connecting the chip to the circuit layer with ^aconductive resin, in addition to the effect of the stress relaxing layer. The semiconductor device does not generate ^areflow failure (at^d) ^{during the} mounting operation, because of the porous stress relaxing layer. ^A(The) failure, such as damage ^{to} (of) the chip ^{was} (is) not generated in the dropping test. Furthermore, the package size can be made (as^d) ^{the} same as the size of the chip, and the package can be made ^{merely} (only) by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 8)

^A(The) semiconductor device 17, which was the same type as indicated in FIG. 4^(a), was prepared by the following manufacturing steps.

The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 2 using alamide non-woven cloth (thermount: made by Du Pont Co.)

[of] 100 μ m thick as the porous body^[i] and a sheet made of rubber modified epoxy resin [of] 30 μ m thick as the adhesive agent and the wafer protecting film. The adhesive sheet was prepared by applying a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone,^{an} ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and^a micro-filler having^a primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) onto^a bed-film, and (drying) the varnish^{was dried}.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test^{to detect} [such as] generation of^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter^{onto} [on] a glass plate [of] 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 [prepared in] the present embodiment has a^{small} warp (as small as) equal to or less than

5 μ m. The semiconductor device 17^a prepared in¹ the present embodiment has a small warp,^a superior thermal cycle resistance, and does not generate^a reflow failure [at]^a during the mounting operation. [The]^A failure, such as damage^{to} of the chip^{was} (is) not generated in the dropping test. Furthermore, the package size can be made [as]^{the} same as the size of the chip, and the package can be made [only]^{merely} by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

10

(Embodiment 9)

[The]^A semiconductor device 17, which was the same type as indicated in FIG. 4,^(a) was prepared by the following manufacturing steps.

15 The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 3 using alamide non-woven cloth (thermount: made by Du Pont Co.) [of] 100 μ m thick as the porous body^(j) and a sheet made of rubber modified epoxy resin [of] 30 μ m thick as the adhesive
20 agent and the wafer protecting film. The adhesive sheet was prepared by applying a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone,^{an} ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was
25 added, and^a micro-filler having^a primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.)

were mixed) onto bed-film, and ^{was dried} (drying) the varnish.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting
5 substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An
10 appearance test such as generation of ^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} [on] a glass plate [of] 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also
15 evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 ¹ [prepared in] the present embodiment has ^{small} a warp [as small as] equal to or less than 5 μm. The semiconductor device 17 ¹ [prepared in] the present embodiment has a small warp, ^a superior thermal cycle
20 resistance, and does not generate ^a reflow failure [at] ^{during the} mounting operation. Because the conductive portions are formed by ^a [the] vapor deposition, ^{the} [the] conductive layer having a high purity can be formed, and ^a electrical resistance is decreased. Therefore, the semiconductor can ^{accommodate} [correspond] ^A
25 ^{an} [to] increasing ^{speed} [velocity] of ^{operation} [electrical signals]. ^A [The] failure, such as damage ^{to} [of] the chip ^{was} [is] not generated in the dropping test. Furthermore, the package size can be made ^{the} [as] same as the size of the chip, and the package can be made ^{only} [only] ^{mainly}

by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 10)

5 ^A
 (The) semiconductor device 17, which was the same type as indicated in FIG. 4, ^(a) was prepared by the following manufacturing steps.

The porous body portions 15 made of porous polytetrafluoroethylene were adhered to the portions ^{of the semiconductor wafer 6} ~~(1)~~ where the electrodes ^{do exist} ~~were~~ not existing on the wafer, of ~~(the semiconductor wafer 6)~~ by heating and pressurizing at 120 °C for 5 seconds. Simultaneously, the wafer protecting film 7, which was as same as the protecting film in the embodiment 1, was adhered to the rear plane of the

10 wafer. Subsequently, the semiconductor wafer was prepared by screen-printing the photosensitive material portions 14 using ^a (the) photosensitive resin (BL-9500: made by Hitachi Kasei Co.) onto the electrodes 5 on the wafer, and drying at 80 °C for 10 minutes.

20 After forming the via-holes by exposing and developing the photosensitive portions, curing was performed at 180 °C for 2 hours. Subsequently, the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same process as the embodiment 2.

25 The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate

FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test (such as ^{to detect} generation of ^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} (on) a glass plate (of) 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also
 10 evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 (prepared in ^{the} present embodiment has a ^{small} warp (as small as) equal to or less than 5 μ m. The semiconductor device 17 (prepared in ^{of} the present embodiment has a small warp. The semiconductor
 15 device is superior particularly in thermal cycle resistance, because the stress relaxing layer is formed of porous polytetrafluoroethylene having a low coefficient of elasticity, and does not generate ^a reflow failure ^{during the} (at) mounting operation, because of ^{the} low humidity
 20 absorbing rate. (The) failure, such as damage (of) the chip ^{was} (is) not generated in the dropping test. Furthermore, the package size can be made (as) ^{the} same as the size of the chip, and the package can be made ^{merely} (only) by dicing the semiconductor wafer of the present embodiment. Therefore, the process
 25 is superior in mass producibility.

(Embodiment 11)

^A (The) semiconductor device 17, which was the same type

as indicated in FIG. 4^(a), was prepared by the following manufacturing steps.

The semiconductor wafer was prepared by the steps of:
 arranging porous body portions made of porous polyimide
 5 having a three dimensional network structure (of) 150 μ
^{thick} ^a ~~whereon~~ thermoplastic polyimide adhesive layer for
 adhering to the semiconductor wafer was formed, on the
 portions of the semiconductor wafer 6⁽¹⁾ where ~~(the)~~ electrodes
 on the wafer ^{do} ~~were~~ ^{exist} ~~not~~ ~~existing~~; arranging the anisotropic
 10 conductive portions 16 on the electrodes on the wafer using
 anisotropic conductive film (ASMAT: made by Nitto Denko
 CO.); and heating and pressurizing. Simultaneously, the
 wafer protecting film 7 made of thermoplastic polyimide
 was adhered to the rear plane of the wafer. Subsequently,
 15 the semiconductor wafer 6 and the semiconductor device 17
 were prepared by the same process as the embodiment 2.

The semiconductor device 17 was mounted on a mounting
 substrate, and a temperature cycle test in the range from
 -55 °C to -125 °C was performed. As the mounting
 20 substrate, a copper clad glass cloth base epoxy laminate
 FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used.
 Furthermore, a reflow test at 240 °C for 5 seconds was
 performed after absorbing moisture in an environment at
 relative humidity 85 % for 48 hours. An appearance test
 25 ^{to detect} ~~(such as)~~ ^a ~~generation of~~ chip crack and the like was performed
 after dropping the semiconductor device at a height of 1
 meter ^{onto} ~~on~~ a glass plate of 5 mm thick. Furthermore, the
 package area versus chip area was evaluated. The amount

of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 [prepared in] the present embodiment has a ^{small} warp [as small as] equal to or less than 5 μ m. The semiconductor device 17 [prepared in] the present embodiment has a small warp. The semiconductor device is superior particularly in thermal cycle resistance by a synergistic effect with the effect of the stress relaxing layer, because making the conductive portion have a low coefficient of elasticity becomes possible by forming the conductive portion between the chip and the circuit layer with an anisotropic conductive material. ^A [The] reflow failure ^{is not generated during the} [a] mounting operation ^(is not) [generated], because of the porous stress relaxing layer. ^A [The] failure, such as damage ^{to} [of] the chip ^{was} [is] not generated in the dropping test. Furthermore, the package size can be made ^{the} [as] same as the size of the chip, and the package can be made ^{merely} [only] by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 12)

A cross sectional view and a perspective view ^{, respectively,} of the semiconductor module of the present invention are indicated in FIG. 7 (a) and (b) ^{, respectively,}. The semiconductor module of the present invention was manufactured by the following process.

The semiconductor devices 17 prepared in the

embodiment 1 and the embodiment 2 were mounted on designated portions of a ^{built} [build]-up mounting substrate having four layered circuits via flux, and ^{the assembly was} treated for reflow at 240 °C for 3 seconds.

- 5 The semiconductor module ^{of} [prepared in] the present embodiment ^{did} [does] not generate any failure at the reflow process in a mounting operation. No failure ^{was} [is] generated in the temperature cycle test.

- 10 (Comparative example 1) ^{as illustrated}
^A [The] semiconductor device ^{then} [indicated] in FIG. 8, was prepared by the following process ⁽¹⁾ and ^{then} evaluated.

After forming the circuit layer by the same method as the embodiment 1, the semiconductor chip 20 was adhered
 15 to the circuit layer with ^a die bonding agent 19. Then, the circuit layer was connected electrically to the chip with ^a gold wire 21 using ultrasonic waves. The connecting portion of the chip and the circuit layer was resin-sealed
 by ^a transfer molding method using an epoxy group sealing
 20 agent. Finally, the semiconductor device was completed by forming the external terminals.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting
 25 substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at

85 °C and a relative humidity of 85 % for 48 hours. An appearance test ^{to detect} (such as) ^a generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} (on) a glass plate (of) 5 mm thick.

5 Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

In case of the present comparative example, the ^{amount of} warp of the package ^{was} (is) large, because the sealing portion is
 10 only on one side of the substrate. Breakage failure (is) ^{occurred} (generated) in the temperature cycle test, because no stress relaxing layer exists. Reflow failure ^{was} (is) generated, because no porous structure for releasing steam exists. The package size becomes larger than the size of the chip,
 15 because the chip is connected to the circuit by wire bonding.

(Comparative example 2)

(The) ^A semiconductor device ^{, as illustrated} (indicated) in FIG. 9, was
 20 prepared by the following process ^{then} (,) and evaluated.

After forming the circuit layer by the same method as the embodiment 1, a relaxing layer was formed thereon by a printing method using ^a silicone group rubber. A silicone group adhesive agent was applied onto the relaxing layer
 25 23, and the semiconductor chip was adhered ^{thereto}. The ^{reference numeral} (numerical) (mark) 26 indicates a gold plated lead. After bonding the chip and the circuit layer ^{using} (by) ultrasonic waves, the bonding portion was sealed with a silicone group sealing agent 22.

Finally, the semiconductor device was completed by forming the external terminals.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from
 5 -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at
 10 85 °C and a relative humidity of 85 % for 48 hours. An appearance test (such as ^{to detect} generation of ^a chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} a glass plate ^(of) 5 mm thick. Furthermore, the package area versus chip area was
 15 evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

In case of the present comparative example, ^a breakage failure ^{occurred} [was generated] in the temperature cycle test, because stresses were concentrated to the lead portion
 20 connecting the chip and the circuit layer by deformation of ^{the} elastomer layer during the temperature cycle test owing to ^{the use of a} (using the) silicone group material for the stress relaxing layer. Failures, such as chip cracks and ^{other problems,} [others] [^] were generated by the dropping test, because no protecting
 25 film was provided ^{at} to the rear plane of the chip. The package size ^{was} [becomes] larger than the size of the chip, because the lead sealing portion ^{was} (is) larger than the chip.

(Comparative example 3)

(The)^A semiconductor device^{, as illustrated} [indicated] in FIG. 10, was prepared by the following process^{then} and evaluated.

Plating bumps 24 are formed at the electrode portions
 5 of the semiconductor wafer. ^{The position} (Position) of the semiconductor wafer is adjusted to match ^{the position of} (with) an epoxy group circuit substrate 25 having the same size as the semiconductor wafer, and the semiconductor wafer is connected electrically to the circuit substrate via the
 10 plating ^{bumps} (bump) 24. A liquid epoxy group sealing agent 22 is filled into an interval between the circuit substrate, and the semiconductor wafer, and ^{is then} cured. After forming the external electrodes 10 on the circuit substrate 25, the semiconductor device was prepared by dicing the
 15 semiconductor wafer.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from -55 °C to -125 °C was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate
 20 FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 °C for 5 seconds was performed after absorbing moisture in an environment at 85 °C and a relative humidity of 85 % for 48 hours. An appearance test ^{to detect} (such as) ^a generation of chip crack and the
 25 like was performed after dropping the semiconductor device at a height of 1 meter ^{onto} (on) a glass plate (of) 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also

evaluated. The results are indicated in Table 1.

In case of the present comparative example, the ^{amounts of} warp of the wafer and the package were large, because the protecting film was not provided onto the rear plane of the chip, and failures, such as chip cracks and ^{other problems,} ~~others~~ were generated by the dropping test. Breakage failures ~~were~~ ^{occurred during} generated in the temperature cycle test, because no stress relaxing film was provided. Failures were generated in the reflow operation, because the sealing portion does not have ^a ~~the~~ porous structure for releasing pressure.

In accordance with the semiconductor devices of the present invention, ^{as} explained in ~~(respective of)~~ the previous embodiments, the failure generation rate at 1000 cycles is low in comparison with the semiconductor devices of the comparative examples 1 ^a and 3, because the stress generated in the external terminals is small ^{due to} ~~(by)~~ the presence of the stress relaxing layer. Because ~~(the)~~ ^a porous body is used as ~~(the)~~ ^a stress relaxing layer, failure ^{during} ~~(at)~~ the mounting reflow ^{does} ~~(is)~~ not ^{occur} ~~generated~~. On account of the presence of the protecting film at the rear plane of the semiconductor chip, the ^{amount of} warp of the package is small in comparison with the comparative examples 1 and 3. Furthermore, in comparison with the comparative examples 1 and 3, the failure generating rate ^{due to} ~~(by)~~ damages, cracks, and the like ^{occurring} in the dropping test is small. ^{any difference in} ~~(The)~~ package area ^{relative} to the chip area is small in comparison with the comparative examples 1 and 2, because the semiconductor wafer, the stress relaxing layer, and the circuit layer are cut

simultaneously along the same plane to^{form} respective units.

The semiconductor device of the present invention comprises a stress relaxing layer between the external terminals and the chip, and an organic protecting film^{is} formed on the rear plane of the chip. Therefore, the^{amount of} warp of the semiconductor device is small, and^{damage to the} damages at edge^{portions} of the chip and cracks are scarcely generated^{during} (in) the dropping test.

The semiconductor device of the present invention^{use of a} comprises the porous stress relaxing layer between the external terminals and the chip. Therefore, breakage at the external terminals^{during the} (by) temperature cycle test after mounting^{occurs} (is) scarcely^{generated}.

Because the stress relaxing layer comprises a three^{time of} dimensional network structure, steam generated at the mounting reflow can be released outside the semiconductor device through the core layer, and swelling and breakage of the substrate, whereon the^{circuits} (circuit) are formed, are seldom generated^{during} (at) the mounting reflow operation.

In accordance with the manufacturing steps of the semiconductor device of the present invention, the package size is^{the} (as) same as the size of the chip, because the assembling operation can be performed simultaneously for^a (the) wafer unit. Therefore, the manufacturing method of the present invention^{has an} (is) advantageous (in) mass producibility.

In accordance with the semiconductor wafer of the present invention, (the)^a semiconductor device having a high

reliability can be manufactured by mass production. The semiconductor module of the present invention has a high reliability, because the semiconductor device of the present invention is mounted.